

CS447 – Networks and Data Communications

Summer 2026

Homework #5 Questions (**SOLUTIONS**)

Your last-three-digits: _____

Submission Due: (each student is required to submit (by email as attached file) your solutions for this homework by **11:00AM on July 16**)

QUESTION #1:

What is the transmission throughput* (not “utilization”) for the following asynchronous transmission configuration? Show your work.

- 1 start-bit
- 10 payload bits
- 1 parity bit
- 2 stop bits (more stop-bits increases the margin for preventing framing errors)
- No errors
- 250 Mbps communication line is used

Note *: the term “throughput” means the actual amount of the information a transmitting host computer will effectively transmit to a receiving host computer.

Solution:

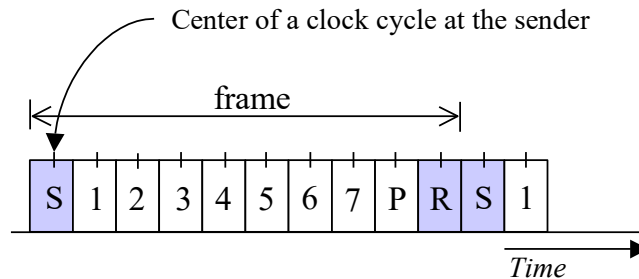
$$\text{Transmission Throughput} = \text{Transmission Rate} \times \text{Utilization}$$

$$U = 10 / (1 + 10 + 1 + 2) = 10 / 14 = 0.714$$

$$\text{Throughput} = (250 \times 10^6) \text{ bps} \times 0.714 = (178.57 \times 10^6) \text{ bps} = \underline{178.57 \text{ Mbps}}$$

QUESTION #2:

In the asynchronous transmission as defined below, what is the minimum receiver-side clock drift rate (in percentage) that can cause a framing error if the receiver's clock is slower than the sender's clock?



Show all your work for full credit.

Solution:

- If the receiver clock is slower than the sender's clock, the sampling point for the stop bit ('R' bit in the figure should skew to the right.
- If the receiver clock skews to the right hand side more than 0.5 bit (a half bit), the receiver will sample the start bit of the next frame, where the start bit is always '1'.
- Knowing that the stop bit can not be '1', the receiver starts looking for the next '0' → '1' signal transition. The next '0' → '1' possibly appears if the first payload bit (sent by the sender) is '0' and if the second payload bit (sent by the sender) is '1'. If these happen, the receiver will take the second payload bit (sent by the sender) as the start of the next frame, which is a framing error.

Conclusion: if the receiver clock skews more than a half bit, the skew can cause a framing error.

From the center of the start bit a frame N, there are:

- 1 half-bit (for the start bit)
- 2 half-bits (for the first payload bit)
- 2 half-bits (for the second payload bit)
- 2 half-bits (for the third payload bit)
- 2 half-bits (for the forth payload bit)
- 2 half-bits (for the fifth payload bit)
- 2 half-bits (for the sixth payload bit)
- 2 half-bits (for the seventh payload bit)
- 2 half-bits (for the parity bit)
- 1 half-bit (to the center of the stop bit)

Total: 18 half-bits

The ratio of the minimum clock skew at the receiver = 1 half-bit/18 half-bits = $1/18 = 0.055$
(5.5%)

QUESTION #3:

Using the following given Message (M) and Key (K), mathematically demonstrate (show the procedures) how CRC error detection can end up with an undetected error using a complete example (“complete” means that you need to show the procedure at both sender and receiver).

- Message (M) = “1 0 1 0 1 0 0” (7 bits)
- Key (K) = “1 1 0 1” (4 bits)

Show all your work.

