CS286 Computer architecture & Organization
Fall 2026
Exercise Questions for October 28, 2026

EXERCISE

Let us assume that we got a pipeline processor (not "super-pipeline") that has a *k*-stage pipeline datapath ($k >> 5$). The processor's delayed branch slot is five cycles.

Suppose that a researcher found that programs for a specific processor have the following properties:

(a) By 72% of chance, the conditional branch instructions take a branch
(b) In 42% probability, there is a data dependency between the instructions in the delay branch slot and a conditional branch instruction (and delayed branch can not be applied because of the dependency)
(c) To simplify your work, let us assume that as long as an instruction in the delayed branch slot has a data dependency with a conditional branch instruction, none of the instructions in the delayed branch can be moved to the behind of a conditional branch instruction

Question:

If the delayed branch should improve the performance of the processor by 6% (i.e., programs run faster by 6% in their execution time), how often conditional branch instructions should appear in the programs?

If you are running out of time, you do not have to finish your calculation (it is OK as long as your formula is correct).

Show all your work.