

CS286 Computer architecture & Organization
Fall 2026
Exercise Questions for October 7, 2026

QUESTION #1

How many instructions will be executed by a processor whose clock cycle rate is 2.0GHz when its CPI is 5.0?

QUESTION #2

For a processor that has a clock cycle rate of 3.2 GHz, how long will it take to finish executing 120 million instructions if the processor's CPI is 2.8?

QUESTION #3

Suppose that we have two processors, A and B. Processor A has a higher clock cycle rate than B. Does this mean that processor A is a better processor than B?

QUESTION #4

Let us assume that we have two processors (Processor A and B). The clock cycle rate and CPI of Processor A are:

**Processor A: Clock cycle rate = 900 MHz.
CPI = 1.2**

The CPI of Processor B is:

Processor B: CPI = 0.7

The two processors have different instruction sets. The average IC for processor A is expected to be 25% smaller than that of Processor B. In order for Processor B to perform at least as fast as Processor A, what should be the clock cycle rate for Processor B?

QUESTION #5

Assuming: n = number of instructions, k = number of stages in a pipeline, and c = clock cycle time. Derive the speed-up factor (speed-up from the scalar architecture) for the following processor architectures (some of the architecture needs more parameters in addition to n , k , and c). It is your responsibility to specify whatever necessary parameter needed for you to specify the speed-up if anything missing.

- (1) Pipeline architecture
- (2) Super-scalar architecture
- (3) Super-pipeline architecture

“the speed-up factor” = “How much is a pipeline processor faster than a scalar processor?”

QUESTION #6

Suppose the branch frequencies (as percentage to all the instructions) are as follows:

Conditional branches:	11%
Jumps and calls:	4%
Conditional branches:	55% are taken

We are examining a ten-phase pipeline processor, in which different instructions require different number of processor cycles to complete (as shown below). Assume that each conditional branch requires eight cycles to complete (the decision of a conditional instruction is made available at the end of the eight cycle). Similarly, each unconditional branch requires six cycles to complete (the decision of an unconditional instruction is made available at the end of the sixth cycle). All other instructions require exactly ten cycles to complete.

Questions: Assuming that only the first pipe stage can always be done independent of whether the branches goes and ignoring other pipeline stalls, (a) how much faster would the machine be without any branch hazards? (b) If the pipeline becomes deeper, what would you expect for the speed up? For (a), show all your work.

QUESTION #7

Assume that all the inputs for each instruction must be available by the beginning of the ID phase and the output from each instruction becomes available at the end of the WB phase, find which of the following four datapath architectures can data hazards for each of RAR, RAW, WAR, and WAW?

- (a) Scalar processors
- (b) Super-scalar processors
- (c) Pipeline processors
- (d) Super-pipeline processors

		1st instruction	
		READ	WRITE
2nd instruction	READ	RAR	RAW
	WRITE	WAR	WAW