

CS447 – Networks and Data Communications

Spring 2024

Exercise Questions on February 5th

EXERCISE #1:

What is the transmission link utilization for the following asynchronous transmission configuration? Show your work.

- 1 start-bit
- 7 payload bits
- 1 parity bit
- 2 stop bits
- No errors

EXERCISE #2:

Suppose that asynchronous serial data transmission is clocked by two clocks (one at the sender and the one at the receiver) that each has a drift of 2.5 minutes in one year. How long a sequence of bits can be sent before possible clock could cause a problem? Assume that a bit waveform will be good if it is sampled within 32% from the center. Assume that the bit samples are taken at the middle of the clock period. Also assume that at the beginning of the start bit the clock and incoming bits are in phase. Show all your work.

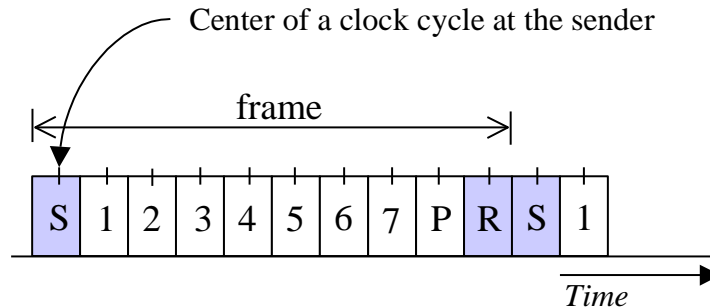
EXERCISE #3:

What is the probability of **non-detectable** error for even parity error detection using the following assumptions (give the formula - you do not have to complete calculation)?

- Bit error rate = 10^{-8}
- Frame size (excluding the start/stop bits) = 8 bits
- Start and stop bits will never cause bit errors.
- Transmission rate = 56.7 Kbps.

EXERCISE #4:

In the asynchronous transmission as defined below, what is the minimum receiver-side clock drift rate that can cause a framing error?



EXERCISE #5:

As we discussed in the lecture on 9/12, the parity error detection is not capable of fixing (correcting) bit errors. Is there any way we can detect some bit errors using parity bits? If no, explain why not. If yes, explain how.