The following is a list of possible questions for our quiz on October 2nd. Some of the questions will not be asked in the quiz. All the questions that will appear in the quiz will appear exactly as shown below (however, numeric parameters may be changed). The quiz is closed textbook, closed notes and closed neighbors. Note that the questions, which did not appear in this quiz, still may appear in the exams. You will find a solution for these questions during lectures.

#1: What does “CPI” stand for? What does it mean?

#2: What is “processor clock cycle”?

#3: What is “processor clock cycle time”?

#4: Show the formula to calculate the execution time (for scalar processors) using, IC (instruction count), R (clock cycle rate), and one more parameter.

#5: Processors with a lower clock rate execute the same binary programs faster than the processors with a higher clock rate. How is this possible?

#6: For the following performance metrics for processors, show which way each metric is better:

- **Execution time**: short long
- **CPU Clock rate**: low high
- **Clock cycle time**: short long
- **CPI**: small large
- **MIPS rate**: small large

#7: What are “scalar datapath processors”?

#8: What are “pipeline datapath processors”?

#9: What are “super-scalar datapath processors”?

#10: What are “super-pipeline datapath processors”?

#11: What are “VLIW datapath processors”? 
#12: What are “vector datapath processors”?

#13: What are “structural hazards”? Show an example of the structural hazard (using assembly instructions).

#14: What are “data hazards”? Show an example of the data hazard (using assembly instructions).

#15: What are “control hazards”? Show an example of the control hazard (using assembly instructions).

#16: What are the four different types of data dependency?

#17: What are the four different types of data dependency?

#18: Show an example of RAR data dependency.

#19: Show an example of RAW data dependency.

#20: Show an example of WAR data dependency.

#21: Show an example of WAW data dependency.

#22: Assume that all the inputs for each instruction must be available by the beginning of the ID phase and the output from each instruction becomes available at the end of the WB phase, find which of the following four datapath architectures can data hazards for each of RAR, RAW, WAR, and WAW?

<table>
<thead>
<tr>
<th>1st instruction</th>
<th>2nd instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>RAR</td>
</tr>
<tr>
<td>WRITE</td>
<td>RAW</td>
</tr>
<tr>
<td>READ</td>
<td>WAR</td>
</tr>
<tr>
<td>WRITE</td>
<td>WAW</td>
</tr>
</tbody>
</table>

#23: What are “static code optimizations”?

#24: What are “dynamic code optimizations”?

#25: Which pipeline hazards is “delayed branches” effective for?

#26: What are the major advantages in “dynamic code optimizations”?

#27: What are the major disadvantages in “dynamic code optimizations”?