(1) What does “ID” stage in a processor datapath do?

The ID (“Instruction Decode”) stage ① identifies the type of the operation and ② sets up inputs (registers and/or constants) to the ALU for the EX stage.

(2) What does “CPI” stand for? What does it mean?

CPI stands for “Cycles Per Instruction”. It represents how many processor cycles are necessary (in average) to finish executing one instruction.

(3) What is “processor clock cycle time”?

The processor clock cycle time is the time for one processor clock at a processor.
(4) For the following performance metrics for processors, show which way each metric is better:

- **Execution time**: short long
- **Clock rate**: low high
- **Clock cycle time**: short long
- **CPI**: small large
- **MIPS rate**: small large

**Note**: the word in the red font is the solution for each term.

(5) What are “super-scalar datapath processors”?

Super-scalar datapath processors are those that have more than one scalar datapath inside of a processor, so that those processors can execute multiple instructions at a time using their multiple scalar datapaths.

![Diagram of clock cycles and instruction execution]

**Note**: either a (correct) solution by English sentence(s) or visualization is good enough for full credit.