The following is a list of possible questions for our quiz on September 27th. Some of the questions will not be asked in the quiz. All the questions that will appear in the quiz will appear exactly as shown below (however, numeric parameters may be changed). The quiz is closed textbook, closed notes and closed neighbors. Note that the questions, which did not appear in this quiz, still may appear in the exams. You will find a solution for these questions during lectures.

**Part I – the “leftover topics” from the previous weeks:**

#1: What is “Moore’s Law”?

#2: What are “super computers” (how fast, what purpose and how large)?

#3: What is “Von-Neumann Architecture”?

#3: What is “Overflow Flag” in a processor (how is it used) for handling operations on two’s complement integers?

**Part II – the new topics from 9/20:**

#5: What are the five basic steps in a processor datapath?

#6: What does “IF” stage in a processor datapath do?

#7: What does “ID” stage in a processor datapath do?

#8: What does “EX” stage in a processor datapath do?

#9: What does “ME” stage in a processor datapath do?

#10: What does “WB” stage in a processor datapath do?

#11: Show the formula to calculate the execution time using, IC (instruction count), R (clock cycle rate), and one more parameter.

#12: Processors with a lower clock rate execute the same binary programs faster than the processors with a higher clock rate. How is this possible?

#13: What are “scalar datapath processors”?

#14: What are “pipeline datapath processors”?
#15: What are “super-scalar datapath processors”?

#16: What are “super-pipeline datapath processors”?

#17: What are “VLIW datapath processors”? 

#18: What are “vector datapath processors”?

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**Part III – the new topics from 9/25:**

#19: What are “structural hazards”? Show an example of the structural hazard (using assembly instructions).

#20: What are “data hazards”? Show an example of the data hazard (using assembly instructions).

#21: What are “control hazards”? Show an example of the control hazard (using assembly instructions).

#22: What are the four different types of data hazards?

#23: Show an example of RAR data hazards.

#24: Show an example of RAW data hazards.

#25: Show an example of WAR data hazards.

#26: Show an example of WAW data hazards.

#27: Assume that all the inputs for each instruction must be available by the beginning of the ID phase and the output from each instruction becomes available at the end of the WB phase, find which of the following four datapath architectures can data hazards for each of RAR, RAW, WAR, and WAW?

<table>
<thead>
<tr>
<th>1st instruction</th>
<th>WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>RAR</td>
</tr>
<tr>
<td>WRITE</td>
<td>WAR</td>
</tr>
<tr>
<td>WRITE</td>
<td>WAW</td>
</tr>
</tbody>
</table>

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CS 286 – Computer Organization & Architecture, Quiz #5, Question List