1. What are the five basic steps (phases) in a processor datapath?

   ![Diagram of processor datapath]

   **Processor**

   - **IF**: Instruction Fetch
   - **ID**: Instruction Decode
   - **EX**: Execution
   - **ME**: Memory access
   - **WB**: Write Back to registers

2. Processors with a lower clock rate execute the same binary programs faster than the processors with a higher clock rate. How is this possible?

   If a processor with a lower clock rate has a lower CPI, the processor can be faster than processors with a higher clock rate.

3. Show the formula to calculate the execution time using, IC (instruction count = ‘n’ in our discussions), R (clock cycle rate), and one more parameter.

   $$\text{Execution Time} = \text{IC} \times \text{CPI} \times \left(\frac{1}{\text{R}}\right)$$
(4) What are “super-scalar datapath processors”?

Super-scalar processors are those processors that have multiple scalar datapath in a processor.

(5) What are “data hazards”? Show an example of the data hazard (using assembly instructions).

Data hazards are the slow-downs caused by “data dependency”, which happens when an instruction must wait for its previous instruction to complete on a common resource (such as registers).

\[
\begin{align*}
&\text{move} \quad \$t1, \$t2: \\
&\text{add} \quad \$t3, \$t1, 5:
\end{align*}
\]