The agenda for CS286 lecture #10 (September 21, 2022):

1. **Pick up:**
   - Attendance card

2. **Quiz #5 is scheduled on next Wednesday (9/28)**

3. **The left-over EXERCISE question (“EXERCISE #8”):**
   
   (a) What is the difference between the 1264th tiniest and the 1265th tiniest numbers (we called the difference “interval”) in IEEE-754 floating point number system (i.e., “single precision IEEE-754 floating point numbers)?

   (b) How many other positive numbers in IEEE-754 floating point number(s) have the same interval to the next tiniest number? (c) Briefly justify your solution.

4. **Introduction to “processor datapath”**
   
   - Quiz #5 question list
   - DataPath.ppt

   The Quiz #5 questions this talk will cover:

   1: What are the five basic steps in a processor datapath?

   #2: What does “IF” stage in a processor datapath do?

   #3: What does “ID” stage in a processor datapath do?

   #4: What does “EX” stage in a processor datapath do?

   #5: What does “ME” stage in a processor datapath do?
#6: What does “WB” stage in a processor datapath do?

#7: What is “PC (Program Counter)” register for?

- Datapath_Architecture.ppt

The Quiz #5 questions this talk will cover:

#8: What does “CPI” stand for? What does it mean?

#9: What is “processor clock cycle”?

#10: What is “processor clock cycle time”?

#11: Show the formula to calculate the execution time (for scalar processors) using, IC (instruction count), R (clock cycle rate), and one more parameter.

#12: Processors with a lower clock rate execute the same binary programs faster than the processors with a higher clock rate. How is this possible?

#13: For the following performance metrics for processors, show which way each metric is better:

- **Execution time**: short long
- **CPU Clock rate**: low high
- **Clock cycle time**: short long
- **CPI**: small large
- **MIPS rate**: small large

#14: What are “scalar datapath processors”?

#15: What are “pipeline datapath processors”?

#16: What are “super-scalar datapath processors”?

#17: What are “super-pipeline datapath processors”?

#18: What are “VLIW datapath processors”?

#19: What are “vector datapath processors”? 