CS286-Computer Organization & Architecture
Possible Quiz Questions (Quiz #7)
For October 8th, 2018

The following is a list of possible questions for our quiz on October 8th. Some of the questions will not be asked in the quiz. All the questions that will appear in the quiz will appear exactly as shown below (however, numeric parameters may be changed). The quiz is closed textbook, closed notes and closed neighbors. Note that the questions, which did not appear in this quiz, still may appear in the exams. You will find a solution for these questions during lectures.

#1: What are “static code optimizations”?

#2: What are “dynamic code optimizations”?

#3: Which pipeline hazards is “delayed branches” effective for?

#4: What are the major advantages in “dynamic code optimizations”?

#5: What are the major disadvantages in “dynamic code optimizations”?

#6: What is “instruction set” (also mention the three factors in “instruction set”)?

#7: What are three components in “instruction set”?

#8: What are “hardwired instructions”?

#9: What are “micro-coded instructions”?

#10: Which of “hardwired instructions” or “micro-coded instructions” has lower CPI?

#11: What are “variable-size instructions”?

#12: What are “fixed-size instructions”?

#13: Which of “variable-size instructions” or “fixed-size instructions” has lower CPI? Why?

#14: What are “(memory) addressing modes”?

#15: What does “CISC” stand for?

#16: What does “RISC” stand for?

#17: For what computer systems, are CISC processors popularly used?

#18: For what computer systems, are RISC processors popularly used?
#19: Compare CISC and RISC processors for the following factors:

<table>
<thead>
<tr>
<th>Factors</th>
<th>CISC</th>
<th>RISC</th>
</tr>
</thead>
<tbody>
<tr>
<td># of available GPRs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Size of the internal cache</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Program size (IC)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock cycle rate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#20: What was the primary performance factor that contributed to the improvement of CPU performance during the first generation (RISC architecture)?

#21: What was the primary performance factor that contributed to the improvement of CPU performance during the second generation (CISC architecture)?

#22: What was the primary performance factor that contributed to the improvement of CPU performance during the third generation (after single-core CISC architecture)?