The following is a list of possible questions for our quiz on March 24th. Some of the questions will not be asked in the quiz. All the questions that will appear in the quiz will appear exactly as shown below (however, numeric parameters may be changed). The quiz is closed textbook, closed notes and closed neighbors. Note that the questions, which did not appear in this quiz, still may appear in the exams. You will find a solution for these questions during lectures.

PART I – to replace the lecture on 3/17

#1: What is “instruction set” (also mention the three factors in “instruction set”)?

#2: What are three components in “instruction set”?

#3: What are “hardwired instructions”?

#4: What are “micro-coded instructions”?

#5: Which of “hardwired instructions” or “micro-coded instructions” has lower CPI?

#6: What are “variable-size instructions”?

#7: What are “fixed-size instructions”?

#8: Which of “variable-size instructions” or “fixed-size instructions” has lower CPI? Why?

#9: What are “(memory) addressing modes”?

#10: What does “CISC” stand for?

#11: What does “RISC” stand for?

#12: For what computer systems, are CISC processors popularly used?

#13: For what computer systems, are RISC processors popularly used?
#14: Compare (which is better?) CISC and RISC processors for the following factors:

<table>
<thead>
<tr>
<th>Factors</th>
<th>CISC</th>
<th>RISC</th>
</tr>
</thead>
<tbody>
<tr>
<td># of available GPRs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Size of the internal cache</td>
<td></td>
<td></td>
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<tr>
<td>Program size (IC)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock cycle rate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#15: What was the primary performance factor that contributed to the improvement of CPU performance during the first generation (RISC architecture)?

#16: What was the primary performance factor that contributed to the improvement of CPU performance during the second generation (CISC architecture)?

#17: What was the primary performance factor that contributed to the improvement of CPU performance during the third generation (after single-core CISC architecture)?

PART II - to replace the lecture on 3/19

#18: Show the memory hierarchy.

#19: What is the trade-off problem in the memory hierarchy?

#20: What is “external memory fragmentation”?

#21: How does “external memory fragmentation” happen?

#22: Why is “memory external fragmentation” a serious problem?

#23: What is “compaction”?

#24: What are the problems in compaction?

#25: Where in the memory hierarchy “virtual memory” exists?

#26: What is “virtual memory”?

#27: What are the three advantages in “virtual memory”?

#28: What is “logical memory address space”?

#29: What is “page fault”? 
#30: What is “valid flag” used in virtual memory for?

#31: Sketch the contents in VMT (virtual memory table).

#32: What is the primary problem in virtual memory?

#33: What is “the internal memory fragmentation”?

#34: How is “dirty flag” used in virtual memory for?

#35: What is “demand paging”? What is the primary advantage?

#36: What is “locality in memory reference”? What are the two different types of “locality”?

#37: What does “TLB” stand for?

#38: In the virtual memory (as we discussed in the classroom), how many disk accesses can happen in the worst case?

#39: Sketch the structure of “segmentation table (or “segmentation descriptor table”)”.

#40: What is the advantage of using segmentation?

#41: How is “segmentation fault” caused?

#42: Which of “page fault” or “segmentation fault” is fatal?